ABSTRACT

A method for fabricating complementary vertical bipolar junction transistors of silicon-on-sapphire in fewer steps than required for true complimentary vertical bipolar junction transistors is disclosed. Initially a thin layer of silicon is grown on a sapphire substrate. The silicon is improved using double solid phase epitaxy. The silicon is then patterned and implanted with P+-type and N+-type dopants. Subsequently a micrometer scale N-type layer is grown that acts as the intrinsic base for both an PNP transistor and as the collector for an NPN transistor. The extrinsic base for the NPN is then formed and the emitter, collector and ohmic contact regions are next selectively masked and implanted. Conductive metal is then formed between protecting oxide to complete the complementary vertical bipolar junction transistors.

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I hereby certify that I deposited the attached paper with the United States Postal Service as "Express Mail Post Office to Addressee" number EV 013492198US in the envelope addressed to: Commissioner of Patents and Trademarks Washington, DC 20231 on 5 MARCH 2002

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